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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/085,164
Filing Date: February 26, 2002
Appellant(s): KELLY ET AL.

Robert C. Klinger
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed August 17, 2009 appealing from the Office action mailed July 24, 2008.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,208,023	Nakayama et al.	03-2001
6,753,597	Crowley et al.	06-2004
5,936,264	Ishinaga	08-1999

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Specification

The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: Specification needs corrections to provide antecedent basis or support to the subject matters of original filed claims 10 and 39.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 10 and 39 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The limitation "further comprising length and width dimensions of approximately .079 milimeters and .050 milimeters, respectively, and a height dimension of approximately .032 milimeters" renders the claim indefinite. It is not clear that "length and width dimensions" and "a height dimension" are the length dimension, the width dimension and the height of which element. It is not clear that length dimension is the length of the input 14 to the output 16 OR the length of the encapsulant 12. It is not clear that the width dimension is the width of the input 14 to the output 16 OR the width of the encapsulant 12. It is not clear that the height dimension is the height of the encapsulant 12 OR the height of the input 14 and output 16.

For the purpose of the examination, the claimed limitation would be interpreted as "the length from the end of the input to the end of the output and the width of the encapsulant dimensions of approximately .079 milimeters and .050 milimeters, respectively, and a height of the encapsulant dimensions of approximately .032 milimeters"

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-8, 12, 13, 15-18 and 42-43 are rejected under 35 U.S.C. 102(e) as being anticipated by Nakayama et al. [U.S. Pat. 6,208,023].

With respect to claim 1, Nakayama et al. (figs. 1a-1c, cols. 9-13) discloses a packaged semiconductor device, comprising:

a semiconductor die (11);

a substrate (12), with the semiconductor die disposed therein;

a plurality of leads (15) coupled to the semiconductor die (11), wherein at least one of said lead has a shaped end proximate the substrate and inherently configured to minimize parasitic capacitance over a predetermined frequency range *[The capacitance is calculated by C=AE/D where A is an area of a conductor, E is a dielectric constant, and D is a distance separating the conductors. In this case, the end of the leads (15) is smaller than the substrate (12), thus the capacitance is smaller if compared to the end of the leads that have the equal or greater size than the substrate. Furthermore, the claim does not disclose what a specified minimize range of the parasitic capacitance over a predetermined frequency]*;

an encapsulant (17) enclosing the semiconductor die (11) and plurality of leads(15), the encapsulant inherently having a consistant dielectric constant over a predetermined frequency range *[The encapsulant (17) is formed of a resin wherein resin materials have the dielectric properties. Furthermore, the term "predetermined frequency range" is not determinant of specifically how the frequency range is determined. The term "predetermined frequency range" is relevant and there is no basic of relevancy. Therefore the encapsulant (17) would have the consistant dielectric constant over predetermined frequency range.]*; and

the encapsulant (17) inherently operable to shunt thermal capacitance and thermal resistance away from the semiconductor die (11). *[It is noted that, resin material are used as insulating materials such as adhesives, insulating films and sealing materials, wherein resin*

materials are excellent in heat resistance, dielectric properties, etc. Therefore, the encapsulant (17, resin) inherently operable to shunt thermal capacitance and thermal resistance away from the semiconductor die.].

With respect to claim 2, Nakayama et al. discloses an I/O common terminal (12, 14) (col. 11, lines 4-11), at least one input terminal (15) and at least one output terminal (15), coupled to the semiconductor die (11) (fig. 1a, col. 9, lines 59-65).

With respect to claim 3, Nakayama et al. discloses that wherein the input terminal (15) and output terminal (15) are positioned orthogonal to the I/0 common terminal (12, 14) (fig. 1c).

With respect to claim 4, Nakayama et al. discloses that the semiconductor die (11) is positioned above the I/0 common terminal (12, 14) (fig. 1c).

With respect to claim 5, Nakayama et al. discloses that the encapsulant (17) forms a substantially hexagonal structure surrounding the I/0 common terminal (12, 14), input terminal (15), and output terminal (15), essentially at right angles with respect to the substrate (fig. 1b).

With respect to claim 6, it is inherent a lead-frame for coupling the input terminal (15) to a circuit and the output terminal (15) to a circuit.

With respect to claim 7, Nakayama et al. discloses that the portion of the lead-frame coupled to each of the input terminal (15) and output terminal (15) possess exposed dovetailed side edges operable to allow epoxy to lock on the sides and top of the exposed edges (fig. 1b).

With respect to claim 8, Nakayama et al. discloses that the an end surface of the input terminal (15) being positioned adjacent and parallel to the side surface of the I/0 common terminal (12, 14), and an end surface of the output terminal (15) being positioned adjacent and parallel to the opposing side surface of the I/0 common terminal, said end surfaces being shaped so as to minimize parasitic capacitance (figs. 1a-1c).

With respect to claims 12 and 43, Nakayama et al. discloses that the packaged semiconductor device used in a surface mount assembly (col. 10, lines 51-63).

With respect to claim 13, Nakayama et al. discloses that the packaged semiconductor device used in an integrated circuit (col. 9, lines 56-58).

With respect to claim 15, Nakayama et al. discloses that the metallization, including a first and second metallization strip (16A), as the means of coupling the input terminal (15) and the output terminal (15) to the semiconductor die (11) (fig. 1b).

With respect to claim 16, Nakayama et al. discloses that a path length from input terminal (15) to the output terminal (15), of a fraction of the wavelength for which frequency the semiconductor device is designed (fig. 1b, col. 11, lines 12-15).

With respect to claim 17, Nakayama et al. discloses that bond wires (16A) as the means of coupling the input terminal (15) and the output terminal (15) to the semiconductor die, the input terminal being coupled to a first end of a first bond wire (16A), a second end of the first bond wire being coupled to the semiconductor die (11), a first end of a second bond wire (16A) being coupled to the semiconductor die (11), a second end of the second bond wire being coupled to the output terminal (15) (fig. 1b).

With respect to claim 18, Nakayama et al. discloses that a path length from the input terminal to the output terminal of a fraction of the wavelength for which frequency the semiconductor device is designed (fig. 1b, col. 11, lines 12-15).

With respect to claim 42, Nakayama et al. (figs. 1a-1c, cols. 9-13) discloses a packaged semiconductor device, comprising:

a semiconductor die (11), a substrate (12), and a plurality of leads (15), wherein at least one of said lead has a shaped end inherently configured to minimize parasitic capacitance over a predetermined frequency range *[The capacitance is calculated by C=AE/D where A is an area of a conductor, E is a dielectric constant, and D is a distance separating the conductors. In this case, the end of the leads (15) is smaller than the substrate (12), thus the capacitance is smaller if compared to the end of the leads that have the equal or greater size than the substrate.*

Furthermore, the claim does not disclose what a specified minimize range of the parasitic capacitance over a predetermined frequency];

a semiconductor die (11) being disposed in the substrate (12);

a coupling means from the plurality of leads (15) to the semiconductor die (11) for providing low capacitance electrical connections which supports device functionality; and

an encapsulation material surrounding the semiconductor die, plurality of leads and coupling means, the encapsulation material making contact with the substrate operable to allow direct dissipation shunting to thermal ground, the encapsulation material having a consistent dielectric constant over the predetermined frequency range *[It is noted that, resin material are used as insulating materials such as adhesives, insulating films and sealing materials, wherein resin materials are excellent in heat resistance, dielectric properties, etc. Therefore, the encapsulant (17, resin) inherently operable to shunt thermal capacitance and thermal resistance away from the semiconductor die. Furthermore, the term "predetermined frequency range" is not determinant of specifically how the frequency range is determined. The term "predetermined frequency range" is relevant and there is no basic of relevancy. Therefore the encapsulant (17) would have the consistant dielectric constant over predetermined frequency range.]*.

Claims 1-4, 8-9, 12-13, 15, 17 and 42-43 are rejected under 35 U.S.C. 102(e) as being anticipated by Crowley et al. [U.S. Pat. 6,753,597].

With respect to claim 1, Crowley et al. (fig. 7, col. 6) discloses a packaged semiconductor device, comprising:

a semiconductor die (32);

a substrate (72), with the semiconductor die disposed therein;

a plurality of leads (38) coupled to the semiconductor die (32), wherein at least one of said lead has a shaped end proximate the substrate and inherently configured to minimize parasitic capacitance over a predetermined frequency range *[The capacitance is calculated by C=AE/D where A is an area of a conductor, E is a dielectric constant, and D is a distance separating the conductors. In this case, the end of the leads (38) is smaller than the substrate (72), thus the capacitance is smaller if compared to the end of the leads that have the equal or greater size than the substrate. Furthermore, the claim does not disclose what a specified minimize range of the parasitic capacitance over a predetermined frequency]*;

an encapsulant (77) enclosing the semiconductor die (32) and plurality of leads (38), the encapsulant inherently having a consistant dielectric constant over a predetermined frequency range *[The encapsulant (77) is formed of a resin wherein resin materials have the dielectric properties. Furthermore, the term "predetermined frequency range" is not determinant of specifically how the frequency range is determined. The term "predetermined frequency range" is relevant and there is no basic of relevancy. Therefore the encapsulant (77) would have the consistant dielectric constant over predetermined frequency range.]*; and

the encapsulant inherently operable to shunt thermal capacitance and thermal resistance away from the semiconductor die (32). *[It is noted that, resin material are used as insulating materials such as adhesives, insulating films and sealing materials, wherein resin materials are excellent in heat resistance, dielectric properties, etc. Therefore, the encapsulant (77, resin) inherently operable to shunt thermal capacitance and thermal resistance away from the semiconductor die.].*

With respect to claim 2, Crowley et al. discloses an I/O common terminal (72) at least one input terminal (38) and at least one output terminal (38), coupled to the semiconductor die (32) (fig. 7).

With respect to claim 3, Crowley et al. discloses that wherein the input terminal (38) and output terminal (38) are positioned orthogonal to the I/0 common terminal (72) (fig. 7).

With respect to claim 4, Crowley et al. discloses that the semiconductor die (32) is positioned above the I/0 common terminal (72) (fig. 7).

With respect to claim 8, Crowley et al. discloses that the an end surface of the input terminal (38) being positioned adjacent and parallel to the side surface of the I/0 common terminal (72), and an end surface of the output terminal (38) being positioned adjacent and parallel to the opposing side surface of the I/0 common terminal, said end surfaces being shaped so as to minimize parasitic capacitance (fig. 7).

With respect to claim 9, Crowley et al. discloses that the leadframe terminal (38) has a rounded shaped on the end surface (fig. 4).

With respect to claims 12 and 43, Crowley et al. discloses that the packaged semiconductor device used in a surface mount assembly (fig. 7).

With respect to claim 13, Crowley et al. discloses that the packaged semiconductor device used in an integrated circuit (col. 1, lines 23-24).

With respect to claim 15, Crowley et al. discloses that the metallization, including a first and second metallization strip (46), as the means of coupling the input terminal (38) and the output terminal (38) to the semiconductor die (32) (fig. 7).

With respect to claim 17, Crowley et al. discloses that bond wires (46) as the means of coupling the input terminal (38) and the output terminal (38) to the semiconductor die, the input terminal being coupled to a first end of a first bond wire (46), a second end of the first bond wire being coupled to the semiconductor die (32), a first end of a second bond wire (38) being coupled to the semiconductor die (32), a second end of the second bond wire being coupled to the output terminal (38) (fig. 7).

With respect to claim 42, Crowley et al. (fig. 7, col. 6) discloses a packaged semiconductor device, comprising:

a semiconductor die (32), a substrate (72), and a plurality of leads (38), wherein at least one of said lead has a shaped end inherently configured to minimize parasitic capacitance over a predetermined frequency range *[The capacitance is calculated by C=AE/D where A is an area of a conductor, E is a dielectric constant, and D is a distance separating the conductors. In this case, the end of the leads (38) is smaller than the substrate (72), thus the capacitance is smaller if compared to the end of the leads that have the equal or greater size than the substrate.*

Furthermore, the claim does not disclose what a specified minimize range of the parasitic capacitance over a predetermined frequency];

a semiconductor die (32) being disposed in the substrate (72);

a coupling means from the plurality of leads (38) to the semiconductor die (32) for providing low capacitance electrical connections which supports device functionality; and

an encapsulation material (77) surrounding the semiconductor die, plurality of leads and coupling means, the encapsulation material making contact with the substrate operable to allow direct dissipation shunting to thermal ground, the encapsulation material having a consistent dielectric constant over the predetermined frequency range *[It is noted that, resin material are used as insulating materials such as adhesives, insulating films and sealing materials, wherein resin materials are excellent in heat resistance, dielectric properties, etc. Therefore, the encapsulant (17, resin) inherently operable to shunt thermal capacitance and thermal resistance away from the semiconductor die. Furthermore, the term "predetermined frequency range" is not determinant of specifically how the frequency range is determined. The term "predetermined frequency range" is relevant and there is no basic of relevancy. Therefore the encapsulant (17) would have the consistant dielectric constant over predetermined frequency range.]*.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 10-11, 14 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakayama et al. [U.S. Pat. 6,208,023] or Crowley et al. [U.S. Pat. 6,753,597].

With respect to claims 10-11 and 39, Nakayama et al. or Crowley et al. substantially discloses all the limitations as claimed above except the length, width, height and the frequency range as claimed by applicant. However, the length, width, height and the operating frequency range would have been obvious to an ordinary artisan practicing the invention because, absent evidence of disclosure of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. *In re Aller*, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). Furthermore, the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are

critical. See *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

With respect to claim 14, Nakayama et al. or Crowley et al. substantially discloses all the limitations as claimed above except the packaged semiconductor device used in an amplifier gain stages. However, it is obvious to the skilled in the art to use the packaged semiconductor device in an amplifier gain stages because it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from the prior art apparatus satisfying the claimed structure limitations. *Ex parte Masham, 2USPQ2d 1647* (1987).

Claims 20-27, 29-32, 34-35, 37-38, and 40-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakayama et al. [U.S. Pat. 6,208,023] in view of Ishinaga [U.S. Pat. 5,936,264].

With respect to claims 20-21, Nakayama et al. does not disclose a light emitting diode as the semiconductor die. However, Ishinaga discloses that it is known in the art a light emitting diode can be used as the semiconductor die (chip) (see col.1, lines 22-27). Therefore, it would have been obvious to the skilled in the art to use the semiconductor die as the light emitting diode as taught by Ishinaga into the device of Nakayama et al. to use as the light emitting diode device.

With respect to claim 22, Nakayama et al. does not disclose a substantially clear epoxy material as the encapsulant. However, Ishinaga discloses that the encapsulant is clear epoxy material (see col. 3, lines 24-27). Therefore, it would have been obvious to the skilled in the art to use clear epoxy material for the encapsulant as taught by Ishinaga into the device of Nakayama et al. in order to allow the light emitted from the LED chip to be transmitted there through.

With respect to claims 23, 26 and 31, Nakayama et al. discloses a cathode (terminal 15) and an anode (terminal 15) as the plurality of leads.

With respect to claim 24, Nakayama et al. discloses that the positioning of the cathode (terminal 15) and the anode (terminal 15) opposite to each other (fig. 1c).

With respect to claim 25, Nakayama et al. discloses an encapsulant (17) with a substantially hexagonal structure around the cathode (terminal 15) and the anode (terminal 15) essentially at right angles with respect to the substrate (12) (fig. 1b).

With respect to claim 27, Nakayama et al. discloses that a shaped end surface of the cathode inherently operable to minimize parasitic capacitance.

With respect to claim 29, Nakayama et al. discloses metallization (16A) as the cathode coupling means to the semiconductor die (11) (fig. 1b).

With respect to claim 30, Nakayama et al. discloses a bond wire (16A) as the means of coupling the cathode to the semiconductor die (11), a first end of the bond wire being coupled to the cathode and a second end of the bond wire being coupled to the semiconductor die (11) (fig. 1c).

With respect to claim 32, Nakayama et al. discloses that a shaped end surface of the anode inherently operable to minimize parasitic capacitance.

With respect to claim 34, Nakayama et al. discloses metallization (16A) as the anode coupling means to the semiconductor die (11) (fig. 1b).

With respect to claim 35, Nakayama et al. discloses a bond wire (16A) as the means of coupling the anode to the semiconductor die (11), a first end of the bond wire being coupled to the anode and a second end of the bond wire being coupled to the semiconductor die (11) (fig. 1c).

With respect to claim 37, Nakayama et al. discloses that the packaged semiconductor device used in an integrated circuit (col. 9, lines 56-58).

With respect to claim 38, Nakayama et al. discloses that the packaged semiconductor device used in a surface mount assembly (col. 10, lines 51-63).

With respect to claim 40, Nakayama et al. (figs. 1a-1c, cols. 9-13) discloses a packaged semiconductor device, comprising:

a substrate (12), a terminal (15), and an encapsulant material (17);

a semiconductor die (11) being disposed in the substrate;

a means coupling the terminal (15) to the semiconductor die (11);

the terminal further comprising a terminal shaped end configured to minimize parasite capacitance over a predetermined frequency range;

a substantially encapsulant (17) for encapsulating the semiconductor die (11), the encapsulant material acting as a thermal shunt to ground operable to decrease thermal capacitance and thermal resistance.

Nakayama et al. does not disclose a light emitting diode as the semiconductor die and a substantially clear epoxy material as the encapsulant. However, Ishinaga discloses that it is known in the art a light emitting diode can be used as the semiconductor die (chip) (see col.1, lines 22-27) and the encapsulant is clear epoxy material (see col. 3, lines 24-27). Therefore, it would have been obvious to the skilled in the art to use the semiconductor die as the light emitting diode as taught by Ishinaga into the device of Nakayama et al. to use as the light emitting diode device. It would have been obvious to the skilled in the art to use clear epoxy material for the encapsulant as taught by Ishinaga into the device of Nakayama et al. in order to allow the light emitted from the LED chip to be transmitted there through.

With respect to claim 41, Nakayama et al. discloses that the packaged semiconductor device used in a surface mount assembly (col. 10, lines 51-63).

Claims 20-24, 26-35, 37-38, and 40-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Crowley et al. [U.S. Pat. 6,753,597] in view of Ishinaga [U.S. Pat. 5,936,264].

With respect to claims 20-21, Crowley et al. does not disclose a light emitting diode as the semiconductor die. However, Ishinaga discloses that it is known in the art a light emitting diode can be used as the semiconductor die (chip) (see col.1, lines 22-27). Therefore, it would have been obvious to the skilled in the art to use the semiconductor die as the light emitting diode as taught by Ishinaga into the device of Crowley et al. to use as the light emitting diode device.

With respect to claim 22, Crowley et al. does not disclose a substantially clear epoxy material as the encapsulant. However, Ishinaga discloses that the encapsulant is clear epoxy material (see col. 3, lines 24-27). Therefore, it would have been obvious to the skilled in the art to use clear epoxy material for the encapsulant as taught by Ishinaga into the device of Crowley et al. in order to allow the light emitted from the LED chip to be transmitted there through.

With respect to claims 23, 26 and 31, Crowley et al. discloses a cathode (terminal 38) and an anode (terminal 38) as the plurality of leads (fig. 7).

With respect to claim 24, Crowley et al. discloses that the positioning of the cathode (terminal 38) and the anode (terminal 38) opposite to each other (fig. 7).

With respect to claim 27, Crowley et al. discloses that a shaped end surface of the cathode inherently operable to minimize parasitic capacitance (fig. 7).

With respect to claims 28 and 33, Crowley et al. discloses that the leadframe terminal (38) has a rounded shape on the end surface (fig. 4).

With respect to claim 29, Crowley et al. discloses metallization (46) as the cathode coupling means to the semiconductor die (32) (fig. 7).

With respect to claim 30, Crowley et al. discloses a bond wire (46) as the means of coupling the cathode to the semiconductor die (32), a first end of the bond wire being coupled to the cathode and a second end of the bond wire being coupled to the semiconductor die (32) (fig. 7).

With respect to claim 32, Crowley et al. discloses that a shaped end surface of the anode inherently operable to minimize parasitic capacitance (fig. 7).

With respect to claim 34, Crowley et al. discloses metallization (46) as the anode coupling means to the semiconductor die (32) (fig. 7).

With respect to claim 35, Crowley et al. discloses a bond wire (46) as the means of coupling the anode to the semiconductor die (32), a first end of the bond wire being coupled to the anode and a second end of the bond wire being coupled to the semiconductor die (32) (fig. 7).

With respect to claim 37, Crowley et al. discloses that the packaged semiconductor device used in an integrated circuit (col. 1, lines 23-24).

With respect to claim 38, Crowley et al. discloses that the packaged semiconductor device used in a surface mount assembly (fig. 7).

With respect to claim 40, Crowley et al. (fig. 7, col. 6) discloses a packaged semiconductor device, comprising:

a substrate (72), a terminal (38), and an encapsulant material (77);

a semiconductor die (32) being disposed in the substrate;

a means coupling the terminal (38) to the semiconductor die (32);

the terminal further comprising a terminal shaped end configured to minimize parasite capacitance over a predetermined frequency range;

a substantially encapsulant (77) for encapsulating the semiconductor die (32), the encapsulant material acting as a thermal shunt to ground operable to decrease thermal capacitance and thermal resistance.

Crowley et al. do not disclose a light emitting diode as the semiconductor die and a substantially clear epoxy material as the encapsulant. However, Ishinaga discloses that it is known in the art a light emitting diode can be used as the semiconductor die (chip) (see col.1, lines 22-27) and the encapsulant is clear epoxy material (see col. 3, lines 24-27). Therefore, it would have been obvious to the skilled in the art to use the semiconductor die as the light emitting diode as taught by Ishinaga into the device of Crowley et al. to use as the light emitting diode device. It would have been obvious to the skilled in the art to use clear epoxy material for the encapsulant as taught by Ishinaga into the device of Crowley et al. in order to allow the light emitted from the LED chip to be transmitted there through.

With respect to claim 41, Crowley et al. discloses that the packaged semiconductor device used in a surface mount assembly (fig. 7).

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakayama et al. [U.S. Pat. 6,208,023] in view of Crowley et al. [U.S. Pat. 6,753,597].

Nakayama et al. substantially discloses all the limitations as claimed above except the configured lead has a rounded shape expanding outward toward the substrate. However, Crowley et al. discloses the leadframe terminal (38) has a rounded shape on the end surface. Therefore, it would have been obvious to the skilled in the art to modify the input and output terminals with the rounded shape on the end surface as taught by Crowley et al. into the device of Nakayama et al. because the round shape

would reduce the material, would improve in the locking strength to the encapsulation and would inherently reduce parasitic capacitance.

Claims 28 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakayama et al. [U.S. Pat. 6,208,023] in view of Ishinaga [U.S. Pat. 5,936,264] as applied to claims 1, 20, 23, 27 and 32 above, and further in view of Crowley et al. [U.S. Pat. 6,753,597].

Nakayama et al. in view of Ishinaga substantially disclose all the limitations as claimed above except a rounded shape on the end surface of the cathode and anode. However, Crowley et al. (fig. 4) discloses the leadframe terminal (38) has a rounded shape on the end surface. Therefore, it would have been obvious to the skilled in the art to modify the input and output terminals with the rounded shape on the end surface as taught by Crowley et al. into the device of Nakayama et al. because the round shape would reduce the material, would improve in the locking strength to the encapsulation and would inherently reduce parasitic capacitance.

(10) Response to Argument

1. The Examiner has Failed to Properly Consider the Specification in Rejecting Claims 10 and 39 for Failing to Comply with the Written Description Requirement.

Appellant (page 19) traverses the 112 second paragraph rejection and submits the claims as written are clear and definite.

This argument is not persuasive because in the drawing of the present invention shows that in figure 2 the length and the width of the encapsulant (12) are .065 and .05, respectively; in figure 3 the length and the height of the input/output terminal (14, 16) are .079 and .01, respectively; in figure 4 the length of the ground (18) is 0.64 and the height of the encapsulant (12) is .032. Therefore, it is not clear that length dimension is the length of the input/output (14/16), the length of the encapsulant (12) or the length of the ground. It is not clear that the width dimension is the width of the input /output (14/16) or the width of the encapsulant (12). It is not clear that the height dimension is the height of the encapsulant (12) or the height of the input/output (14/16). Moreover, the width of the encapsulant (12) is .050 not .065 as claimed by Appellant in claims 10 and 39.

2. The Examiner has failed to properly construe all claims, and particularly Claim 40.

Appellant (pages 19-20) argues that the construction of the claims adopted by the Examiner is incorrect, and is used to improperly reject the claims. Specifically, the Examiner refused to enter the proposed amendment to the claim 40.

This argument has been considered and the 112 second paragraph has been removed.

3. Claims 1-8, 12, 13, 15-18 and 42-43 are not anticipated by or obvious in view of Nakayama, as it fails to disclose each element of the claimed invention.

• Appellant (page 20) argues that "Nakayama fails to disclose at least a lead having a shaped end to minimize parasitic capacitance over a predetermined frequency range and an encapsulant having a consistent dielectric constant over a predetermined frequency range, which are disclosed in the specification of the pending application as described above".

This argument is not persuasive because any dielectric material between two conductors would provide the capacitance. And the capacitance is calculated by C=AE/D where A is an area of a conductor, E is a dielectric constant, and D is a distance separating the conductors. In this case, the end of the leads (15) is smaller than the substrate (12), thus the capacitance is smaller if compared to the end of the leads that have the equal or greater size than the substrate. Furthermore, the claim does not disclose what a specified minimize range of the parasitic capacitance over a predetermined frequency. Therefore, Nakayama meets and anticipates the claim language.

• Appellant (page 21) also argues that "the claim limitation at issue is not the **size** of the leads, but the **shaped end**. A review of the leads 15 of Nakayama reveals that they are all rectangular, with sharp comers. As taught in the specification of the pending application at paragraph [0024], the "anode 71 has a shaped end surface operable to minimize parasitic capacitance." That shaped end surface noticeably contains no sharp corners".

This argument is not persuasive because the leads 15 of Nakayama are all rectangular, with sharp comers but the area of rectangular is smaller than the area of the conductive substrate (12). Therefore, it will produce small capacitance compare to the capacitance with the lead shape equal to the conductive substrate. Also, there is no basis for this statement (That shaped end surface noticeably contains no sharp corners).

• Appellant (page 22) argues that "Nakayama fails to disclose the encapsulant having a consistant dielectric constant over predetermined frequency. Nakayama does not discuss or even mention the dielectric constant of the molding resin 17, and the Examiner's hindsight attempt to assert inherency fails to provide any basis in fact and/or technical reasoning to reasonably support the determination that a second allegedly inherent characteristics necessarily flows from the teachings of Nakayama".

This argument is not persuasive because the encapsulant (17) is formed of a resin wherein resin materials have the dielectric properties. The term "predetermined frequency range" is not determinant of specifically how the frequency range is determined. The term "predetermined frequency range" is relevant and there is no basic of relevancy. Furthermore, the material (epoxy resin, see col. 1, and lines 46-48) for the encapsulant formed by Nakayama is the same material as the present claimed invention. Therefore the encapsulant (17) of Nakayama would have the consistant dielectric constant over predetermined frequency range.

- Appellant (pages 22-23) argues that "Nakayama fails to disclose that claim 8 includes "the packaged semiconductor device as recited in Claim 3, further comprising an end surface of the input terminal(s) being positioned adjacent and parallel to the side surface of the I/O common terminal, and an end surface of the output terminal(s) being positioned adjacent and parallel to the opposing side surface of the I/O common terminal, said end surfaces being shaped so as to minimize parasitic capacitance." In regards to claim 8, the Examiner does not rely on inherency .et. Nakayama do not incorporate any of the features disclosed in the specification that are utilized to minimize parasitic capacitance, which are equally applicable to claims 1 and 8".

This argument is not persuasive because Nakayama et al. clearly discloses that the end surface of the input terminal (15) being positioned adjacent and parallel to the side surface of the I/0 common terminal (12, 14), and an end surface of the output terminal (15) being positioned adjacent and parallel to the opposing side surface of the I/0 common terminal (figs. 1a-1c). The end surfaces being shaped so as to minimize parasitic capacitance (see the rejection in claim 1 and the argument above).

- Appellant (page 23-24) argues that "Nakayama fails to disclose that claim 16 includes the "packaged semiconductor device as recited in Claim 15, further comprising a path length from input terminal to the output terminal, of a **fraction of the wavelength for which frequency the semiconductor device is designed."** Likewise, claim 18 includes the "packaged semiconductor device as recited in Claim 17, further comprising

a path length from the input terminal to the output terminal of a **fraction of the wavelength for which frequency the semiconductor device is designed."** In fact, Nakayama discloses no dimensions for the subject path length, only that parasitic inductance is reduced so as to allow operation over a wide frequency range without thermal damage. Such inductance-related losses from operation over a wide frequency range would not be present in a device operating at a fixed frequency of operation. Likewise, nothing in Nakayama indicates that the frequency of operation should be limited so as to limit a path length from input terminal to the output terminal to a fraction of the wavelength for which frequency the semiconductor device is designed".

This argument is not persuasive because the claim does not recited the frequency of operation should be limited so as to limit a path length from input terminal to the output terminal to a fraction of the wavelength for which frequency the semiconductor device is designed or the dimensions for the subject path length. Moreover, since Appellant does not specify what value of the claiming frequency is, thus any type of frequency would meet this limitation.

4. Claims 1-4, 8-9, 12-13, 15, 17 and 42-43 are not anticipated by Crowley, because Crowley fails to disclose each element of the claimed inventions.

- Appellant (page 25) argues that "Crowley fails to disclose at least a lead having a shaped end to minimize parasitic capacitance over a predetermined frequency range and an encapsulant having a consistent dielectric constant over a predetermined

frequency range, which are disclosed in the specification of the pending application as described above".

This argument is not persuasive because any dielectric material between two conductors would provide the capacitance. And the capacitance is calculated by C=AE/D where A is an area of a conductor, E is a dielectric constant, and D is a distance separating the conductors. In this case, the end of the leads (38) is smaller than the substrate (72) (see fig. 7), thus the capacitance is smaller if compared to the end of the leads that have the equal or greater size than the substrate. Crowley (fig. 4) also discloses the leads (38) have a round shaped as claimed by appellant. Furthermore, the claim does not disclose what a specified minimize range of the parasitic capacitance over a predetermined frequency. Therefore, Crowley meets and anticipates the claim language.

• Appellant (page 25) argues that "there is no indication that the two apparently slightly-rounded corners Crowley are anything other than a draftsman's choice".

This argument is not persuasive because the drawing is a prior art.

• Appellant (page 26) argues that "Crowley fails to disclose the encapsulant having a consistant dielectric constant over predetermined frequency".

This argument is not persuasive because the encapsulant (77, col. 2, lines 38-45) is formed of a epoxy resin wherein epoxy resin materials have the dielectric properties. The term "predetermined frequency range" is not determinant of specifically

how the frequency range is determined. The term "predetermined frequency range" is relevant and there is no basic of relevancy. Furthermore, the material (epoxy resin) for the encapsulant formed by Crowley is the same material as the present claimed invention. Therefore the encapsulant (77) of Crowley would have the consistant dielectric constant over predetermined frequency range.

• Appellant (page 28) argues that "Crowley fails to disclose a path length from input terminal to the output terminal to a fraction of the wavelength for which frequency the semiconductor device is designed".

This argument is not persuasive because the claim does not recited the frequency of operation should be limited so as to limit a path length from input terminal to the output terminal to a fraction of the wavelength for which frequency the semiconductor device is designed or the dimensions for the subject path length. Moreover, since Appellant does not specify what value of the claiming frequency is, thus any type of frequency would meet this limitation.

5. Claims 10-11, 14 and 39 are not unpatentable over Nakayama or Crowley, as neither reference discloses each element of the claims.

• Appellant (page 28) argues that claims 10-11, 14 and 39 are allowable at least for the reasons that the claims depend from an allowable base claim.

This argument is not persuasive because the base claim is still rejected (see rejection and argument above).

6. Claims 20-27, 29-32, 34-35, 37-38 and 40-41 are not unpatentable over Nakayama in view of Ishinaga, because they fail to disclose each element of the claimed inventions.

- Appellant (page 29) argues that "Ishinaga, like Nakayama, fails to even mention the dielectric constant of the encapsulant, much less that it should be consistent over a predetermined frequency range".

This argument is not persuasive because Nakayama inherently discloses the encapsulant having a consistant dielectric constant over predetermined frequency (see the rejection and the argument above).

- Appellant (page 29) argues that "in Claim 20, further comprising a substantially clear epoxy material as the encapsulant. Hence, not only must the encapsulant have a consistent dielectric constant over the predetermined frequency range, it must also be substantially clear. The failure of either Nakayama or Ishinaga to disclose an encapsulant having a consistent dielectric constant over the predetermined frequency range, much less the effect that the color of the encapsulant must be taken into consideration".

This argument is not persuasive because Ishinaga discloses that the encapsulant is clear epoxy material (see col. 3, lines 24-27). The material (clear epoxy resin) for the encapsulant formed by Ishinaga is the same material as the present claimed invention claimed. Therefore the encapsulant of Ishinaga would have the consistant dielectric constant over predetermined frequency range.

7. Claim 9 is not unpatentable over Nakayama in view of Crowley, as they fail to disclose each element of the claimed invention.

• Appellant (page 30) argues that "there is no rounded shape expanding toward the substrate disclosed in Crowley".

This argument is not persuasive because Crowley clearly discloses the lead (38) has a rounded shape expanding toward the substrate (see fig.4).

8. Claims 28 and 33 are not unpatentable over Nakayama in view of Ishinaga and further in view of Crowley, as they fail to disclose each element of the claimed inventions.

• Appellant (pages 30-31) argues that "Crowley discloses an encapsulated circuit, there is again no mention that the encapsulant has a consistant dielectric constant over a predetermined frequency range. As with Nakayama and Ishinaga, Crowley fails to even mention the dielectric constant of the encapsulant".

This argument is not persuasive because Crowley inherently discloses the encapsulant having a consistant dielectric constant over predetermined frequency (see the rejection and the argument above).

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

HP

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